ARCHITECTURE OF A SCALABLE AND ADAPTABLE PATTERN GENERATOR ALIGNED FOR BUILT-IN SELF-TEST APPLICATIONS

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A diverse array of patterns is crucial in various fields, including machine learning, cryptography, and VLSI testing. Diversity in machine learning improves training accuracy; in cryptography, it enhances resistance to attacks; and in VLSI testing, it increases fault coverage and minimises the risk of test escapes. Conventional Linear Feedback Shift Registers (LFSRs) are commonly utilised for pattern generation; however, their configurability and flexibility are often insufficient, which restricts their effectiveness in diverse applications. This study presents a configurable and parameterizable pseudo-random pattern generator (PRPG) utilising LFSR architecture, intended for application as a Test Pattern Generator (TPG) within Built-In Self-Test (BIST) frameworks. The proposed design accommodates various LFSR configurations, such as Fibonacci, Galois, Reseeding, and Complete LFSRs, and can generate patterns derived from both primitive and non-primitive polynomials. The evaluation encompassed polynomial degrees from 4 to 319, illustrating its adaptability. The primary architectural contributions consist of the integrated execution of various LFSR modes within a singular hardware block, along with its capacity to accommodate an extensive array of testing scenarios. Experimental validation utilising Cadence tools on a 45nm technology node confirms the design's functionality and efficiency, establishing it as a reliable solution for contemporary testing and pattern generation requirements.

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