DESIGN OF LOW POWER CORDIC BASED FFT STRUCTURE

Nancharaiah Vejendla[1], Rongali Durgaprasad [2]
1 Associate Professor, Department of Electronics and Communication Engineering
2 PG Student, Department of Electronics and Communication Engineering
1, 2 Lendi Institute of Engineering and Technology, Affiliated by jntu kakinada
Vizianagaram,India

In digital signal processing systems, we are substantially use the fast Fourier transform algorithm, consequently, the evolution of a low power CORDIC structure based on FFT structures. In real time signal processing this type of structure are highly desirable, by using algorithm R2DIF (radix two DIF). We propose a low power FFT processor used for FPGA devices. In this propose by decreasing the memory footprints of complex twiddle factors of multipliers the power consumption and chip-area is reduced. To multiply the complex twiddle factors without requiring memory blocks, a multiplication technique is used based on the combinations of a unrolled coordinate rotations digital computers (CORDIC) and the canonical sign digits based binary expressions (CSDBE) is utilized. For optimize the multiplication of constants in the structure we use CSDBE technique. We tested the proposed low power CORDIC FFT processor with a help of a Xilinx Virtex-7 FPGA. The proposed design enhances performance, latency, capacity, accuracy, and energy consumption of computing on FPGA's devices over the existing design, according to experimental data.

 ISBN: - 978-81-968898-2-1