STATIC TIMING ANALYSIS IN VLSI DESIGN

Pragati Agarwal Research Scholar
Electronics and Communication Engineering, IFTM University, Moradabad, India
Neelu Trivedi Associate Professor
IFTM University, Moradabad, India
Rohit Kumar Gupta Associate Professor
Kalyan Singh Government Medical College,Bulandshahr, India
Rajat Agarwal MBBS
Shri Ram Murti Smarak Institute of Medical Sciences,Bareilly, India

When we move towards the nanometer designs, the interconnections between the semiconductor devices. At this level the performance of the design is affected by the metal interconnects. Earlier, dynamic simulations of the gate-level net-list were performed, which has become a problem for the complex designs of today. Nowadays, we have billions of transistors in a typical digital circuit. Doing verification dynamically where a stimulus is given to the input signals and the outputs are observed, could take several days and even weeks to complete the verification process. The dynamic timing simulation depends on the coverage of the used test-bench and the quality for verification. The parts on which the stimuli are applied are tested while the remaining parts remain untested. Therefore, verification of timing analysis of a digital design is done with the help of a technique known as Static Timing Analysis (or STA). With the introduction of static timing analysis (STA), use of dynamic simulation has been limited to check the functionality of the RTL Design.

In static timing analysis (STA), the timing analysis is done statically, which means that there is no dependency on the signal applied to the input pins of the design. Static timing analysis (STA) is an exhaustive technique and uses mathematical techniques. If the definitions of input clock and of the external environment are set, then static timing analysis (STA) could validate whether that design could work at the desired speed or not.

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