COMPARATIVE STUDY OF PERIPHERAL AND INTERSTITIAL MACRO PLACEMENT AND ITS IMPACT ON TIMING AND POWER PERFORMANCE

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In this modern era with the introduction of IoT the demand for multifunctionality chips has shown significant growth and the target can be achieved with the proper use of predefined and pre-verified functional blocks in SoCs. Macros which are defined and pre-verified functional block that serve specific purpose plays a pivotal role in the chip design process. With the efficient placement and use of macros the efficiency and performance of the chip can be enhanced. This paper provides an in-depth analysis of macro placement strategies and their impact on QoR, ranging from timing to power efficiency and congestion at different stages of the physical design flow. In the proposed work we have conducted a comparative analysis between two major macro placement approaches: interstitial and peripheral placement. With keeping in mind QoR metrics such as WNS, TNS, utilization, congestion, and leakage power. We have shed light into the interplay between macro placement techniques and their impact on QoR metrics such as WNS, TNS, utilization and leakage power.

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